Claims

What is claimed is:

1. A comparator circuit comprising:

an evaluation element; and

at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs having non-complementary structures relative to one another and being adapted to receive respective first and second input signals, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of the first and second input signals.

2. The comparator circuit of claim 1 wherein the first and second input signals comprise non-complementary input signals.

3. The circuit of claim 1 wherein the variable parameter for a given one of the input legs comprises a variable resistance.

4. The comparator circuit of claim 1 wherein the variable parameter for a given one of the input legs comprises a variable current.

5. The comparator circuit of claim 1 wherein the variable parameter for a given one of the input legs comprises a variable voltage.

6. The comparator circuit of claim 1 wherein the evaluation element comprises a memory cell.

7. The comparator circuit of claim 6 wherein the evaluation element comprises a random access memory (RAM) cell.

8. The comparator circuit of claim 1 wherein the evaluation element comprises a differential amplifier.

9. The comparator circuit of claim 1 wherein at least one of the first and second input legs comprises a weighted array of transistors, each of the transistors in the weighted array adapted to receive a particular portion of an input signal applied to that leg.

10. The comparator circuit of claim 9 wherein the weighted array comprises an array of transistors digitally sized in width in accordance with a corresponding relationship between portions of a digital input signal.

11. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, and wherein the first and second inputs each comprise a digital word having a plurality of bits, and wherein each transistor of the associated weighted array of transistors is adapted to receive as an input a corresponding bit of a given one of the digital words.

12. The comparator circuit of claim 11 wherein the transistors of the weighted array are weighted in accordance with factors 2^0, 2^1, . . . 2^{n-1} in width and the weighted array is adapted to receive a corresponding input signal comprising an n-bit digital word.

13. The comparator circuit of claim 9 wherein the weighted array comprises an additional transistor having an input adapted to receive an offset signal, the offset signal being configured so as to ensure a predictable output result if comparison of the first and second inputs would otherwise result in an unpredictable output.

14. The comparator circuit of claim 1 being implemented in a pipelined structure, the first and second input legs each being adapted to receive multi-bit digital words as the respective first and second input signals, the pipelined structure having a plurality of stages with each stage involving a comparison of designated portions of the multi-bit digital words.

15. The comparator circuit of claim 14 wherein the first and second input legs are adapted to receive m×n-bit digital words, and the pipelined structure has m stages with each stage configured to perform an n-bit comparison of a selected portion of the digital words.

16. The comparator circuit of claim 14 wherein the pipelined structure comprises an N-tree to N-tree structure.

17. The comparator circuit of claim 14 wherein the pipelined structure comprises an N-tree to P-tree structure.

18. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, the first and second input signals each comprising a digital word having a plurality of bits, wherein each transistor of a given one of the weighted arrays is adapted to receive as an input a corresponding bit of a given one of the digital words, each of the transistors in each of the weighted arrays having a substantially equal width such that comparison of the digital words implements a majority rule function.

19. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, the first and second input signals each comprising one or more balanced analog input signal pairs, inputs of parallel transistors in a particular one of the weighted arrays being adapted to receive respective signals of a given one of the pairs, each of the transistors in each of the weighted arrays having a substantially equal width such that the comparator circuit is configured to provide an analog common mode comparison.

20. The comparator circuit of claim 1 wherein each of the first and second input legs comprises a weighted array of transistors, the first and second input signals each comprising one or more analog input signals, inputs of parallel transistors in a particular one of the weighted arrays being adapted to receive corresponding ones of the analog input signals, each of the transistors in

each of the weighted arrays having a substantially equal width such that the comparator circuit is configured to provide an analog common mode comparison.

21. The comparator circuit of claim 1 being a first comparator circuit coupled with a second comparator circuit having an evaluation element and at least first and second input legs each coupled to a corresponding one of a first node and a second node of the evaluation element of the second comparator circuit, the first input leg of the first comparator being adapted to receive an input signal representing a first bound, the second input leg of the second comparator being adapted to receive an input signal representing a second bound, the second input leg of the first comparator and the first input leg of the second comparator both being adapted to receive another input signal, the first and second comparator circuits collectively being adapted to generate an output indicative of whether or not the other input signal falls within the first and second bounds.

22. The comparator circuit of claim 1 having at least a third input leg coupled to the first node of the evaluation element adjacent the first input leg, the third input leg having associated therewith a variable parameter having a value that is a function of a corresponding input signal, the evaluation element being adapted to perform a comparison of the result of an addition of at least first and third inputs applied to the respective first and third input legs with a second input applied to the second input leg.

23. The comparator circuit of claim 1 having a first plurality of input legs including the first leg coupled to the first node of the evaluation element, and a second plurality of input legs including the second input leg coupled to the second node of the evaluation element, each of the input legs having associated therewith a variable parameter having a value that is a function of a corresponding input signal, the evaluation element being adapted to perform a comparison of the result of an addition of a first plurality of inputs applied to respective ones of the first plurality of input legs with the result of an addition of a second plurality of inputs applied to respective ones of the second plurality of input legs.

24. The comparator circuit of claim 22 being implemented as a serial adder-binary search (SA-BS) circuit having a finite state machine being adapted to generate inputs for application to the second input leg in accordance with a binary search process, so as to determine the result of an addition of inputs applied to the first and third input legs.

25. The comparator circuit of claim 24 wherein the SA-BS circuit is one of m SA-BS circuits each being adapted to perform an n-bit function so as to implement an m×n-bit serial adder.

26. The comparator circuit of claim 1 wherein a first set of input legs associated with the first node of the evaluation element and a second set of input legs associated with the second node of the evaluation element are adapted to receive a substantially constant current, for at least a designated period of time, so as to implement an analog adder function.

27. The comparator circuit of claim 23 further comprising a multiplexer being adapted to select a particular pair of the inputs for propagation to an output thereof so as to implement an add-compare-select (ACS) function.

28. The comparator circuit of claim 23 being one of a plurality of ACS circuits, each being adapted to compare at least a first pair of inputs with a second pair of inputs, the plurality of ACS circuits being implemented in a layered architecture having a plurality of layers including a final layer having a single one of the ACS circuits, the layered architecture being adapted such that winning pairs from one layer are compared against one another at a subsequent layer until a final winning pair is identified.

29. The comparator circuit of claim 28 further comprising an associated adder being adapted to perform an addition of the final winning pair of inputs.

30. The comparator circuit of claim 1 being a first comparator circuit and further comprising at least a second comparator circuit coupled in parallel therewith so as to implement a coupled memory cell comparator.

31. The comparator circuit of claim 30 further comprising a third comparator circuit having first and second input legs each coupled to a corresponding one of a first and second input leg of one of the first comparator circuit and the second comparator circuit.

32. The comparator circuit of claim 1 wherein the first and second input legs each have associated therewith a plurality of mask inputs, the mask inputs being adapted to receive mask signals operative to configure the first and second input legs so as to implement a masking of corresponding portions of the first and second input signals from consideration in the comparison performed by the evaluation element.

33. The comparator circuit of claim 1 wherein the first and second input legs each comprise a plurality of variable resistances arranged in a stack, each of the variable resistances having an input associated therewith, and the evaluation element comprises a differential amplifier.

34. The comparator circuit of claim 1 wherein at least one of the first and second input legs includes an offset signal input, the offset signal input being adapted to introduce signal information into the comparator circuit.

35. The comparator circuit of claim 34 wherein the signal information comprises carry input signal information.

36. A comparator circuit comprising:

an evaluation element; and

at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs being adapted to receive

respective first and second non-complementary input signals, each of the first and second input legs having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of the first and second input signals.

37. An integrated circuit comprising:

at least one comparator circuit, the comparator circuit comprising an evaluation element, and at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs having non-complementary structures relative to one another and being adapted to receive respective first and second input signals, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of first and second input signals.

38. A comparator circuit comprising:

an evaluation element; and

at least first and second input legs each coupled to a corresponding one of a first and second node of the evaluation element, the first and second input legs being adapted to receive respective first and second input signals, each of the first and second input legs having associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals, the evaluation element being adapted to perform a comparison of the first and second input signals, wherein outputs of the comparator circuit are isolated from corresponding output nodes of the evaluation element such that the comparison is substantially independent of asymmetry associated with the outputs of the comparator circuit.

39. A comparator circuit comprising:

a plurality of add-compare-select (ACS) circuits implemented in a layered architecture having a plurality of layers including a final layer having a single one of the ACS circuits and an associated adder being adapted to perform an addition of a final winning pair of

inputs, the layered architecture being configured such that winning pairs from one layer are compared against one another at a subsequent layer until the final winning pair is identified.

40. A circuit comprising at least first and second input legs, the first and second input legs having non-complementary structures relative to one another, each of the non-complementary structures having associated therewith a variable parameter having a value that is a function of a corresponding input signal, a difference in the variable parameters associated with the first and second input legs being detectable in the circuit.

41. The circuit of claim 40 further comprising an evaluation element, wherein the first and second input legs are each coupled to a corresponding one of a first and second node of the evaluation element, the evaluation element being adapted to perform a comparison of first and second input signals applied to the respective first and second input legs.